Transistor Hybrid equivalent circuit and Single stage CE Amplifier

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Transistor Configuration

On the basis of common terminal between input and output

- **CB mode:** **Base is common between input and output**
- **CE Mode:** **Emitter is common between input and output**
- **CC mode:** **Collector is common between input and output**

On the basis of Biasing

- **R-R Bias: Cut-off mode**

  Input/Ist Junction- Reverse Bias; Output/IInd Junction- Reverse Bias.

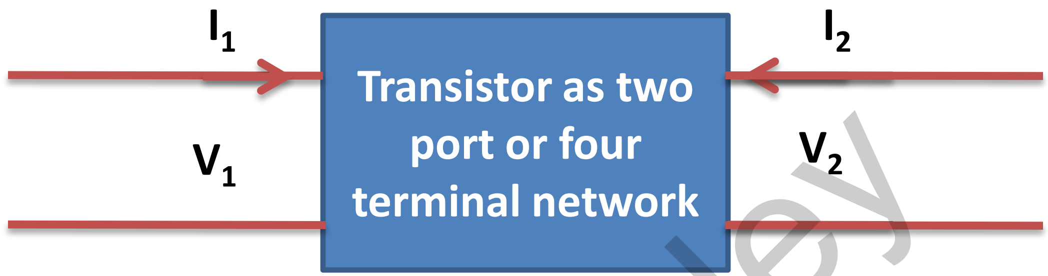
- **F-R Bias: Active mode**

  Input/Ist Junction- Forward Bias; Outtput/IInd Junction- Reverse Bias.

- **F-F Bias: Saturation mode**

  Input/Ist Junction- Forward Bias; Output/IInd Junction- Forward Bias.

Transistor Current and Voltage: Two-Port Network



I_1: Input current
V_1: Input voltage

I_2 : Output current
V_2: Output voltage

- Relation in V and I provides: Four type of parameters

  Impedance Z, Admittance Y, Hybrid h, Inverse-hybrid g

Both currents and Both voltages can be related by four types

Transistor Current and Voltage: Two-Port Network

1. Transistor V-I relation in terms of Impedance Parameters

$$V_1 = f(I_1, I_2)$$
$$V_2 = f(I_1, I_2)$$

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}$$

$$V_1 = Z_{11}I_1 + Z_{12}I_2 \qquad V_2 = Z_{21}I_1 + Z_{22}I_2$$

2. Transistor V-I relation in terms of Admittance Parameters

$$I_1 = f(V_1, V_2)$$
$$I_2 = f(V_1, V_2)$$

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} Y_{11} & Y_{12} \\ Y_{21} & Y_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}$$

$$I_1 = Y_{11}V_1 + Y_{12}V_2 \qquad I_2 = Y_{21}V_1 + Y_{22}V_2$$

Transistor Current and Voltage: Two-Port Network

3. Transistor V-I relation in terms of hybrid Parameters

$$V_1 = f(I_1, V_2)$$
$$I_2 = f(I_1, V_2)$$

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

$$V_1 = h_{11} I_1 + h_{12} V_2 \qquad I_2 = h_{21} I_1 + h_{22} V_2$$

4. Transistor V-I relation in terms of Inverse hybrid Parameters

$$I_1 = f(V_1, I_2)$$
$$V_2 = f(V_1, I_2)$$

$$\begin{bmatrix} I_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} g_{11} & g_{12} \\ g_{21} & g_{22} \end{bmatrix} \begin{bmatrix} V_1 \\ I_2 \end{bmatrix}$$

$$I_1 = g_{11} V_1 + g_{12} I_2 \qquad V_2 = g_{21} V_1 + g_{22} I_2$$

Transistor hybrid equivalent circuit

Transistor V-I relation in terms of hybrid Parameters

$$V_1 = f(I_1, V_2)$$
$$I_2 = f(I_1, V_2)$$

$$\begin{bmatrix} V_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} h_{11} & h_{12} \\ h_{21} & h_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ V_2 \end{bmatrix}$$

$$V_1 = h_{11}I_1 + h_{12}V_2 = h_i I_1 + h_r V_2$$

$$I_2 = h_{21}I_1 + h_{22}V_2 = h_f I_1 + h_o V_2$$

Four characteristic curves, Four hybrid Parameters

Input characteristic curve: Graph between V_1 and I_1 at constants V_2.

h_i: input impedance or resistance

$$h_i = \left(\frac{\partial V_1}{\partial I_1}\right)_{\Delta V_2 = 0}$$

Transistor hybrid equivalent circuit

Reverse voltage transfer characteristic:
Graph between V_1 and V_2 at constants I_2.

h_r: reverse voltage gain/ratio

$$h_r = \left(\frac{\partial V_1}{\partial V_2}\right)_{\Delta I_2 = 0}$$

Forward current transfer characteristic :
Graph between I_2 and I_1 at constants V_2.

h_f: forward current gain/ratio

$$h_f = \left(\frac{\partial I_2}{\partial I_1}\right)_{\Delta V_2 = 0}$$

Output characteristic: Graph between I_2 and V_2 at constants I_1.

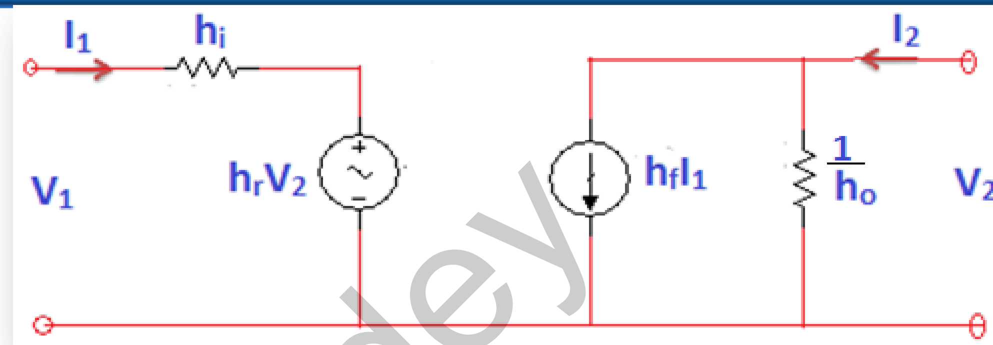
h_0: output admittance

$$h_o = \left(\frac{\partial I_2}{\partial V_2}\right)_{\Delta I_2 = 0}$$

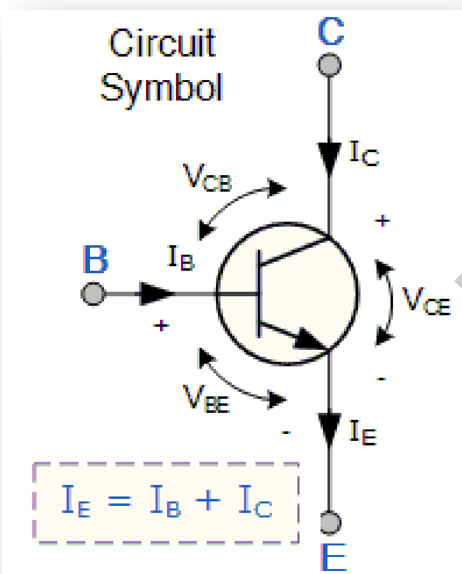
Transistor hybrid equivalent circuit

$$V_1 = h_i I_1 + h_r V_2$$

$$I_2 = h_f I_1 + h_o V_2$$

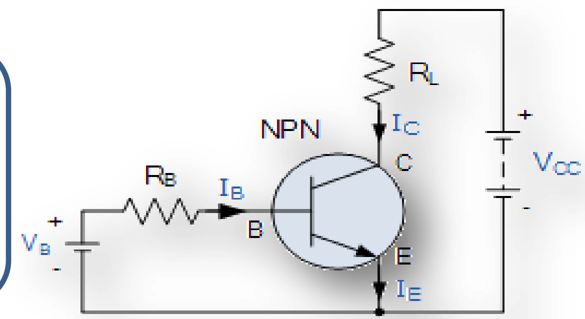


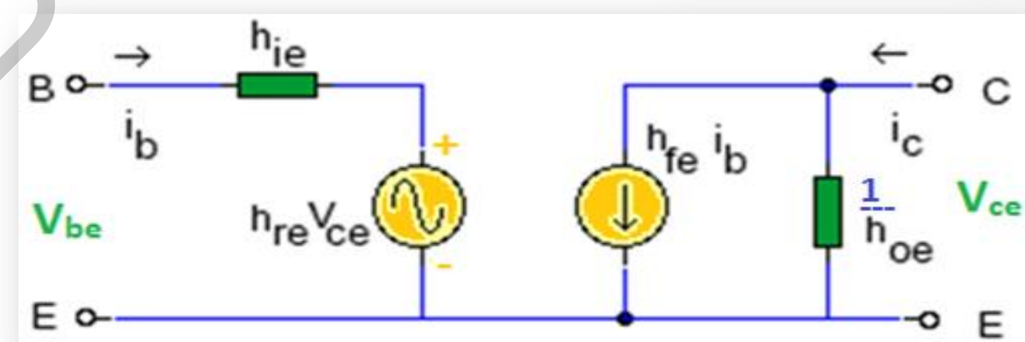
Transistor hybrid equivalent circuit in CE mode



$$V_{be} = h_{ie} i_b + h_{re} V_{ce}$$

$$i_c = h_{fe} i_b + h_{oe} V_{ce}$$





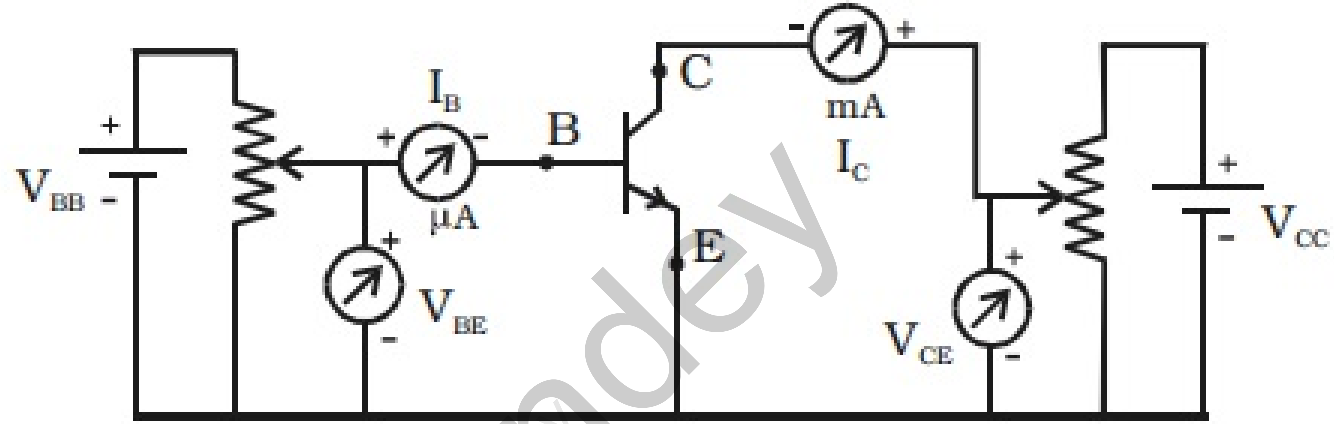
Characteristic curves in CE mode

$h_{ie} \sim k\Omega$

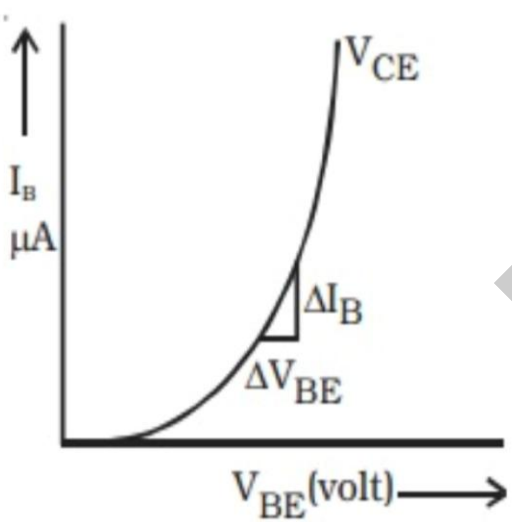
$h_{re} \sim 10^{-4}$

$h_{fe} \sim 50\text{-}500$

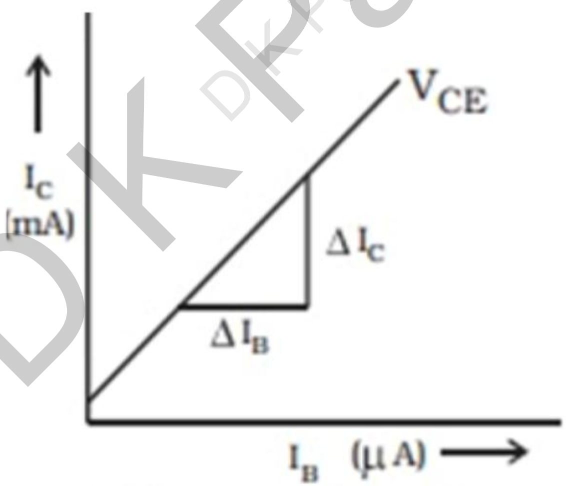
$h_{oe} \sim 10^{-5}\ \Omega^{-1}$



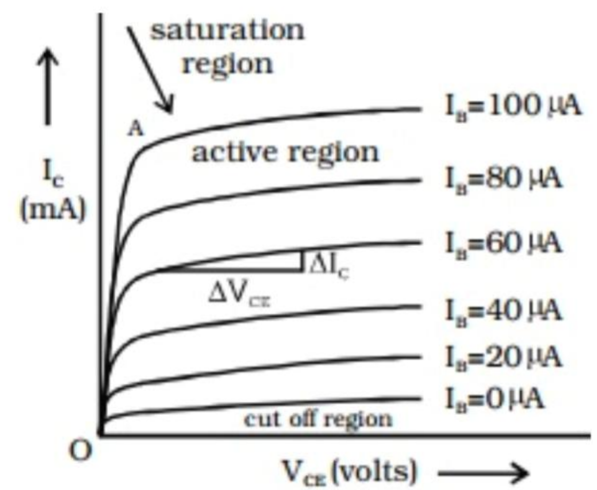
Transistor Biasing in CE Mode



Input Characteristic



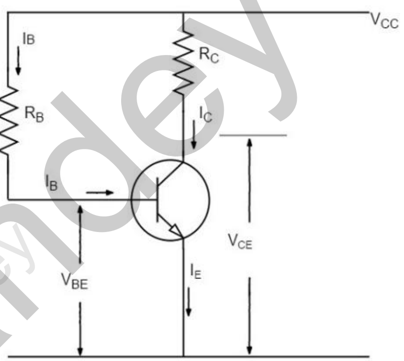
Forward Current transfer Characteristic

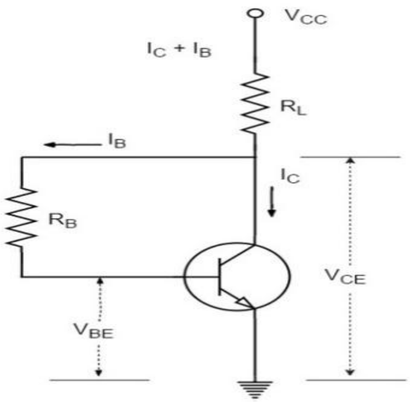


Output Characteristic

Biasing of transistor

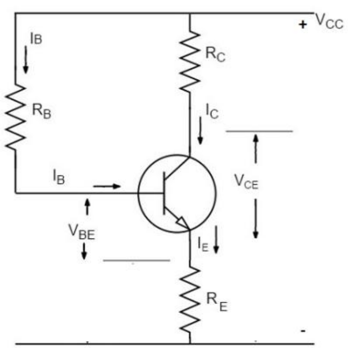
Biasing is the process by which a proper DC source (V_{BB}, V_{CC})/potential difference can be provided to the input and output circuit of the transistor.

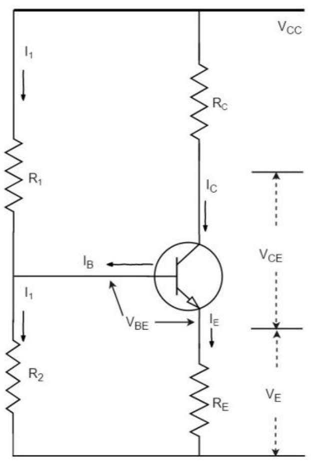




Type of Biasing

1. **Fixed Bias or Base Bias**
2. **Collector to Base Bias**
3. **Emitter Bias or Self Bias**
4. **Potential Divider Bias**





Correct Biasing

1. **Q-point should not vary.**
2. **Stability factor should be minimum.**
3. **There should not be thermal runaway.**

Stability Factor and Thermal runaway

$$S = \frac{dI_C}{dI_{C0}} = \frac{1+\beta}{1-\beta\left(\frac{dI_B}{dI_c}\right)}$$

$$I_C = \beta I_B + (1+\beta) I_{C0}$$

S :Minimum; Stability: High

1. β varies for same type/number of transistor
2. Temperature causes change in leakage current

1. T: increases ; I_{CO}: Increases; I_C: Increases
2. If I_C : increases then temp: increases and further I_{CO}: Increases
3. I_C and Temp : continuously increases
4. Due to heating: the self destruction of unstabilized transistor is known as thermal runaway.

Q-point or operating point

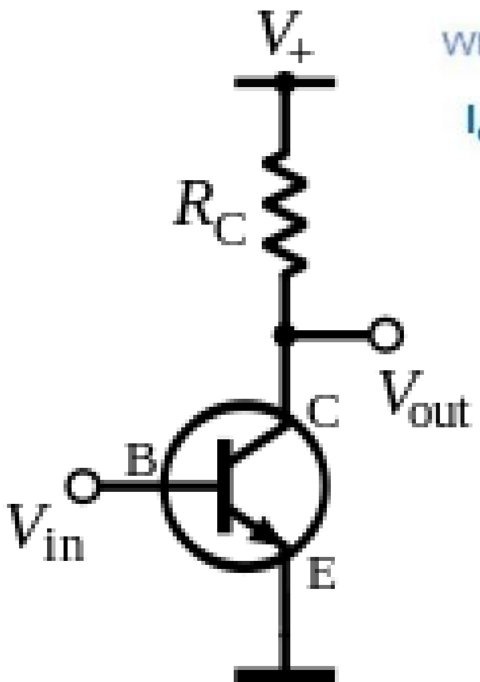
The operating point of a device, also known as a bias point, quiescent point or Q-point, is the steady-state DC voltage or current at a specified terminal of an active device such as a transistor with no input signal applied.

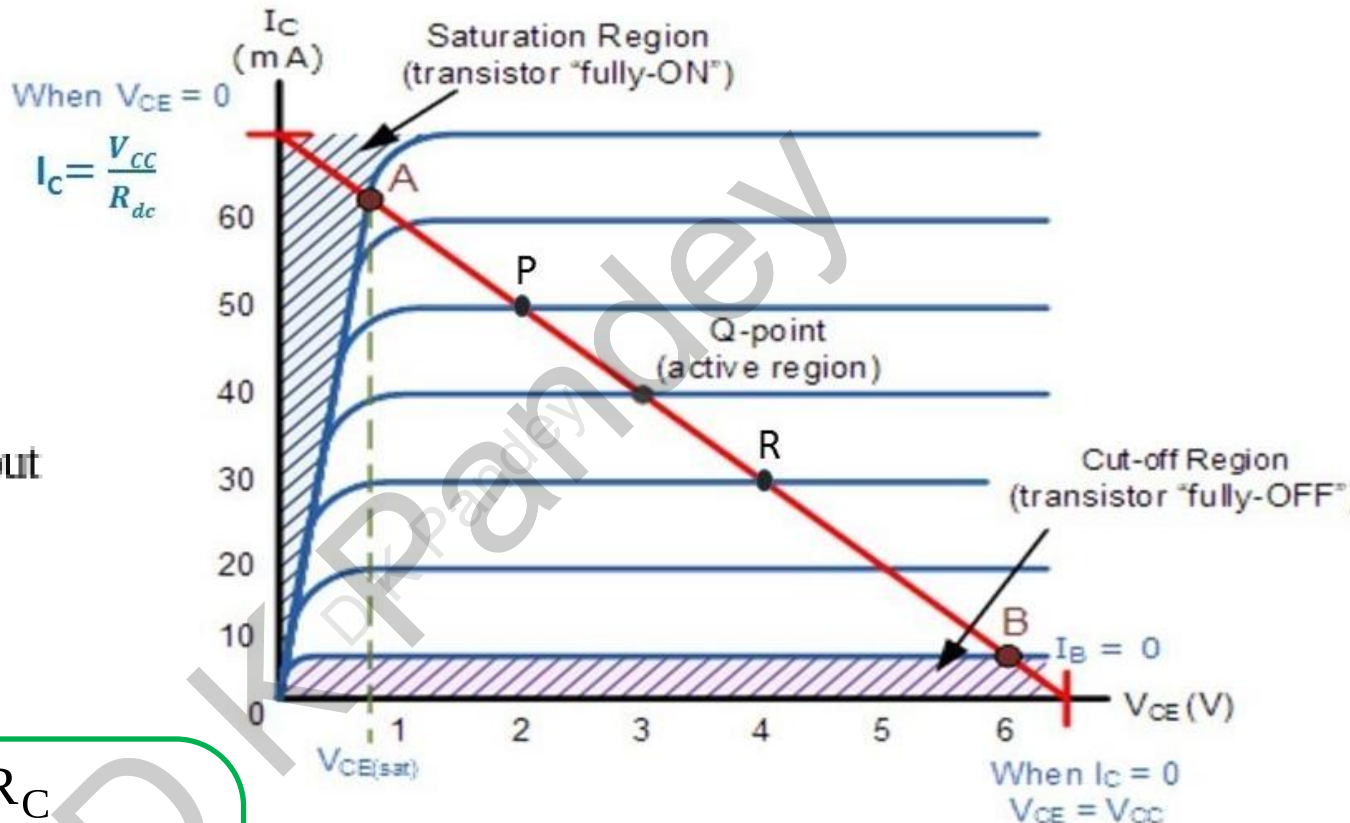
Q-point is an acronym for **Quiescent point**. Q-point is the operating point of the transistor **(I_{CQ},V_{CEQ})** at which it is biased. The concept of Q-point is used when transistor act as an amplifying device and hence is operated in active region of input output characteristics. To operate the BJT at a point it is necessary to provide voltages and currents through external sources.

Why stabilization of operating point is needed?

In practice the **operating point varies shifts due to drift in temperature** e.t.c. **As temperature increases I_{co}, β, V_{be} gets affected**. The reverse saturation current almost doubles for every 10 degree rise in collector junction temperature. The base to emitter voltage decreases by 2.5 milli volts for every one degree rise in temperature. **Hence the operating point should be stabilized against the variations in temperature** so that it remains stable. To achieve this biasing circuits are introduced.

Q-point or operating point : DC Load Line





$$V_{CC} = V_{CE} + I_C R_C$$

$$I_C = \left(-\frac{1}{R_C}\right) V_{CE} + \frac{V_{CC}}{R_C}$$

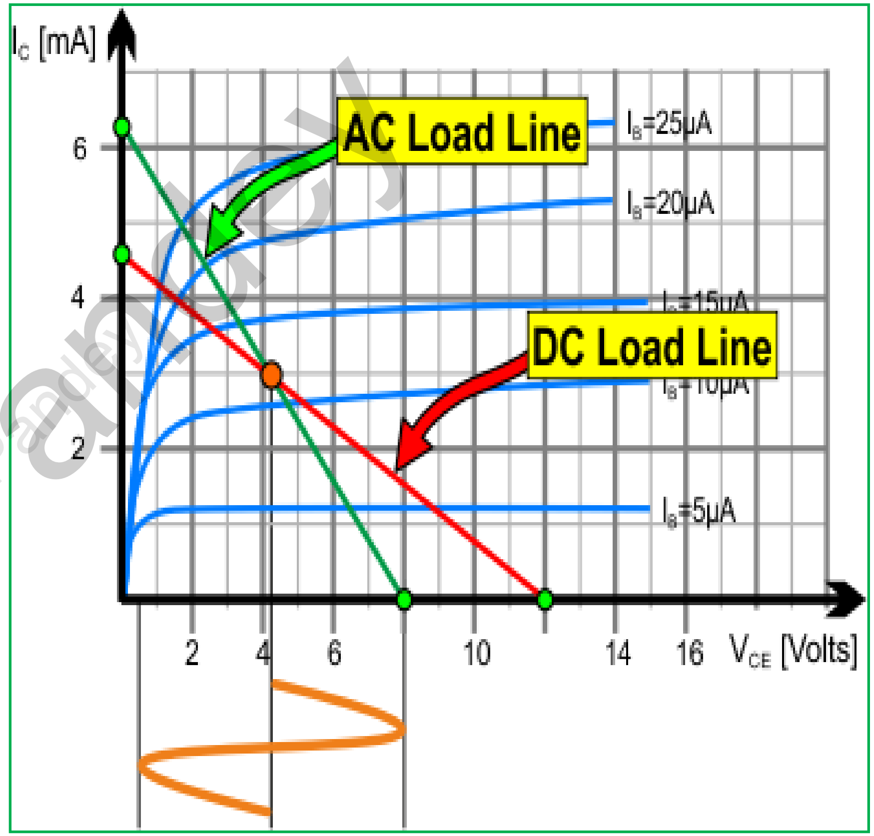
Best Q-point position

$$V_{CE} = \frac{V_{CC}}{2}$$

1. (V_{cc}, 0) is cut off point where transistor enters in to cut off region from active region
2. (0, V_{cc}/R_c) is saturation point where the transistor enters saturation region.

Q-point or operating point : AC Load Line

It is straight line through the quiescent operating point but having slope corresponding to AC load resistance. The AC load seen by the amplifier is different from the DC load, and so the slope of AC load line is different. The AC load line indicates the maximum possible output-voltage swing, called the peak-to-peak output voltage (V_{pp}) for a given amplifier configuration. This maximum V_{pp} is often referred to as the compliance of the amplifier.



Q-point or operating point : AC Load Line

When an a.c. signal causes the change in output voltage and current of amplifier, the Q-point shifts up and down along a line. This line is known as a.c. load line.

The cut-off point of a.c. load line is given by

$$V_{CE}\,(\text{cut off}) = V_{CEQ} + I_{CQ}\, R_{ac}$$

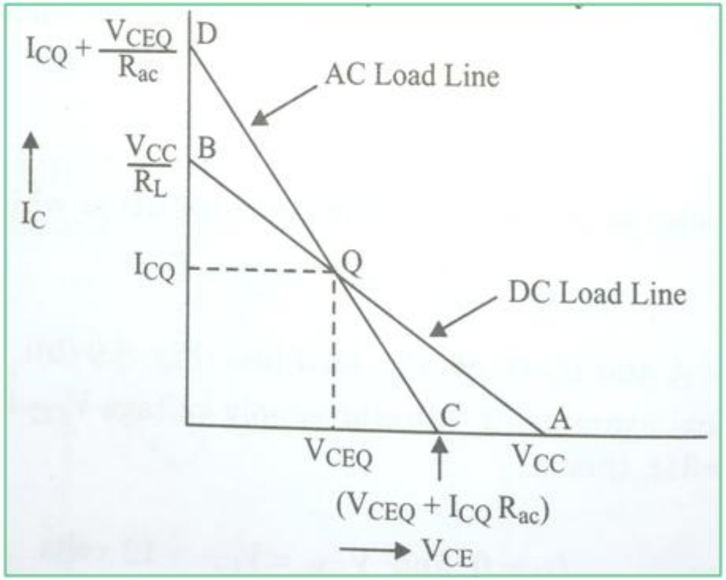
where R_{ac} is the a.c. load resistance. Saturation point is given by

$$I_{C(\text{sat})} = I_{CQ} + \frac{V_{CEQ}}{R_{ac}}$$

These points have been represented by C and D, respectively in fig. whereas CQD represents the a.c. load line.

The slope of a.c. load line is given by

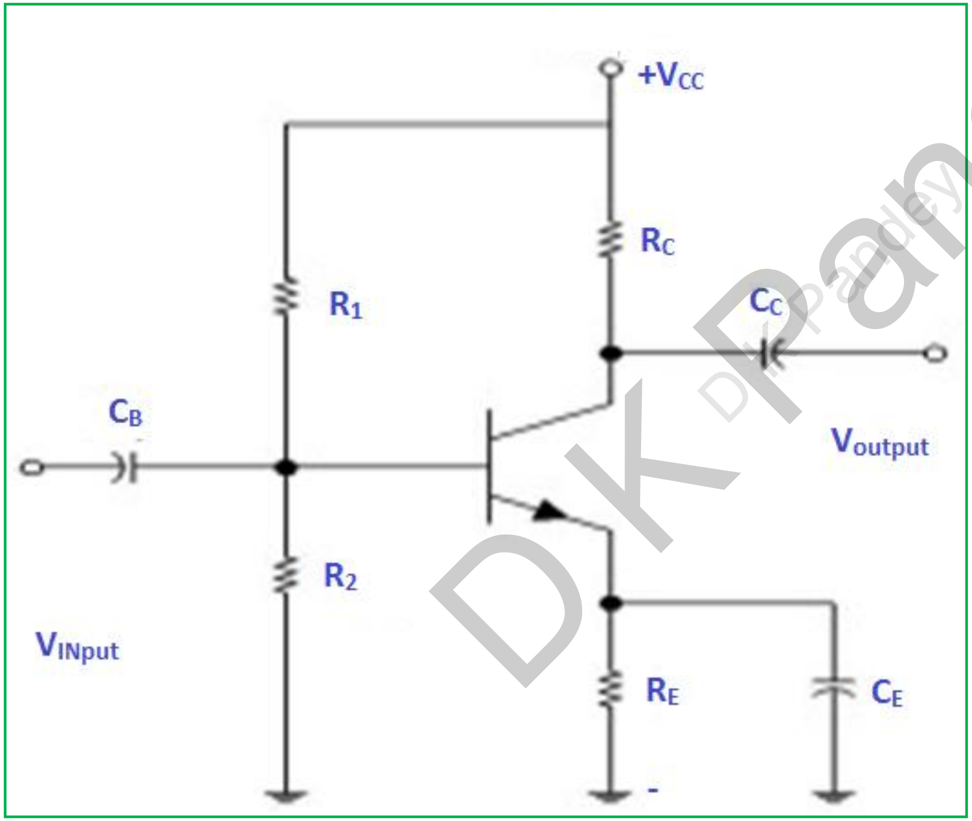
$$y = -\frac{1}{R_{ac}}$$



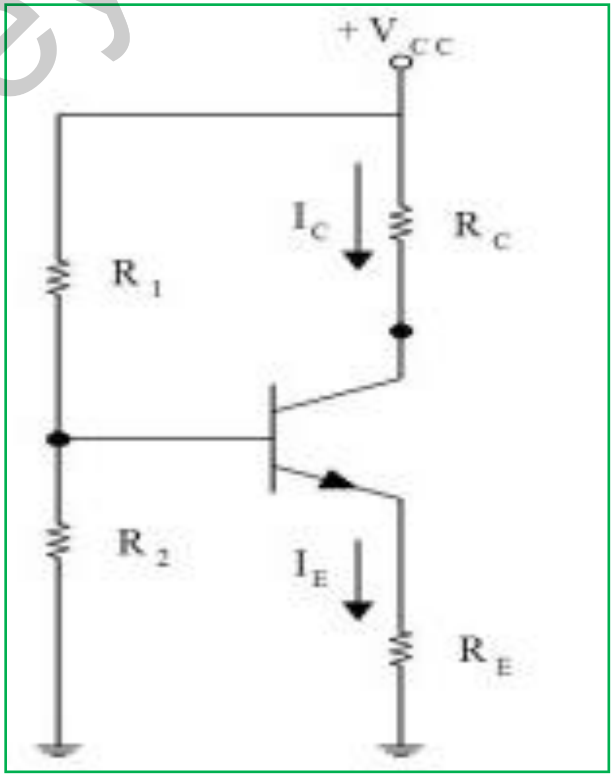
$$Rac = R_C \,\text{II}\, R_1 = \frac{R_C R_1}{R_C + R_1}$$

Potential Divider Biasing of Transitor

The **voltage divider bias method** is the most prominent method for of providing biasing and stabilization. Here, two resistors R_1 and R_2 are employed, which are connected to V_{CC} and provide biasing. The resistor R_E employed in the emitter provides stabilization.



Potential Divider biasing of transistor



DC equivalent of Potential Divider biasing of transistor

Potential Divider Biasing of Transitor

Voltage across R_2 = V_2=V_{Th}

$$V_2 = \left(\frac{V_{CC}}{R_1 + R_2}\right) R_2$$

Applying KVL in base emitter junction

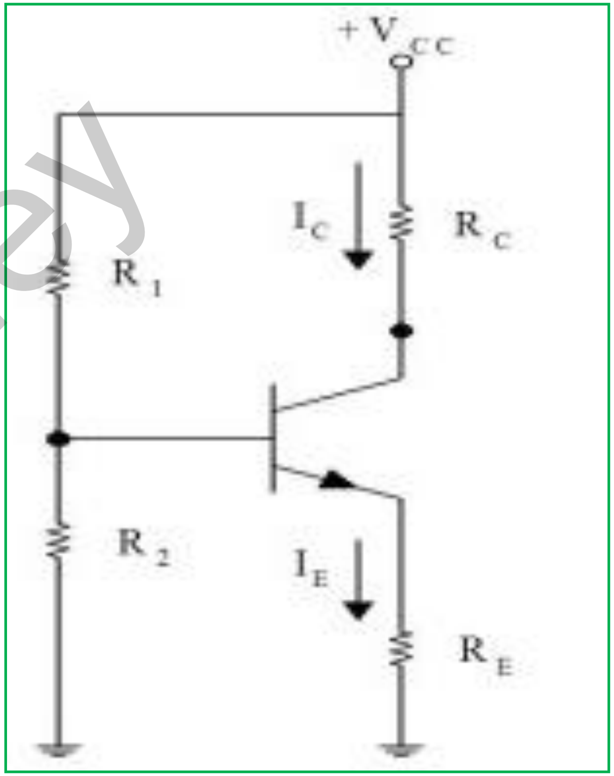
$$V_2 = V_{BE} + V_E$$

$$V_2 = V_{BE} + I_E R_E$$

$$I_E = \frac{V_2 - V_{BE}}{R_E}$$

Since $I_E \approx I_C$,

$$I_C = \frac{V_2 - V_{BE}}{R_E}$$



From the above expression, it is evident that I_C doesn't depend upon β. V_{BE} is very small that I_C does not get affected by V_{BE} at all. Thus I_C in this circuit is almost independent of transistor parameters and hence good stabilization is achieved. **Stability factor =1**

Potential Divider Biasing: Numerical

Example. *Find the operating point for the bias circuit shown in fig. if* $V_{BE} = 0.5V$ *and* $\beta = 40$.

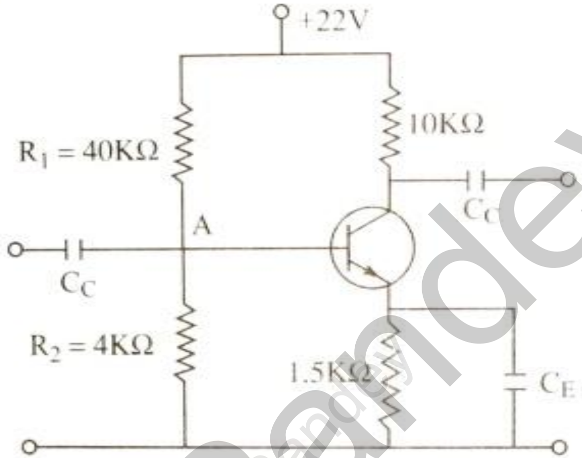


Fig.

Solution : Open circuit voltage across the terminals A, B

$$V_{oc} = \frac{R_2}{R_1 + R_2} V_{cc}$$

$$= \frac{4 \times 10^3}{(40+4) \times 10^3} \times 22 = 2 \text{ volt}$$

Therefore, collector current

$$I_c = \frac{V_{oc} - V_{BE}}{R_E} = \frac{2 - 0.5}{1.5 \times 10^3} = \mathbf{1\ mA}$$

Voltage across collector and emitter

$$V_{CE} = V_{CC} - I_C (R_C + R_E)$$

$$= 22 - 1 \times 10^{-3} (10 + 1.5) \times 10^3$$

$$= \mathbf{10.5\ V}$$

Potential Divider Biasing: Numerical

Example: Convert this previous emitter-bias example to voltage divider bias. Given that-

$$\beta = 100 \qquad I_E \approx I_C = 1mA \qquad V_{CC} = 10V \qquad V_{BB} = 1.5V \quad R_E = 470\Omega$$

$$\beta = 100 \qquad I_E \approx I_C = 1mA \qquad V_{CC} = 10V \qquad V_{BB} = 1.5V \quad R_E = 470\Omega$$

$$R_B = \beta\left[\frac{V_{BB} - V_{BE}}{I_E} - R_E\right] = 100\left[\frac{1.5 - 0.7}{0.001} - 470\right] = 33k$$

$$V_{BB} = Vth = 1.5V$$

$$R_B = Rth = 33k$$

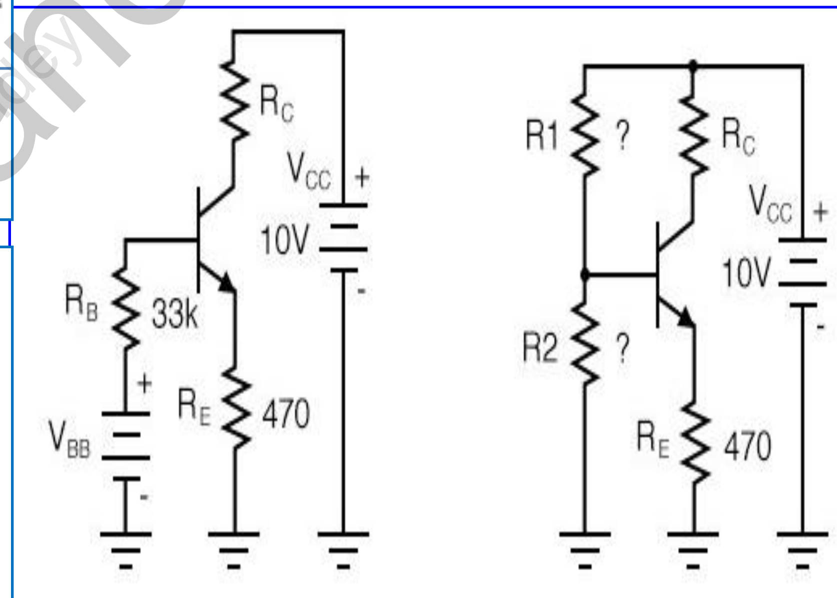
$$R1 = Rth\frac{V_{CC}}{Vth}$$

$$R1 = 33k\frac{10}{1.5} = 220k$$

$$\frac{1}{R2} = \frac{1}{Rth} - \frac{1}{R1}$$

$$\frac{1}{R2} = \frac{1}{33k} - \frac{1}{220k}$$

$$R2 = 38.8k$$

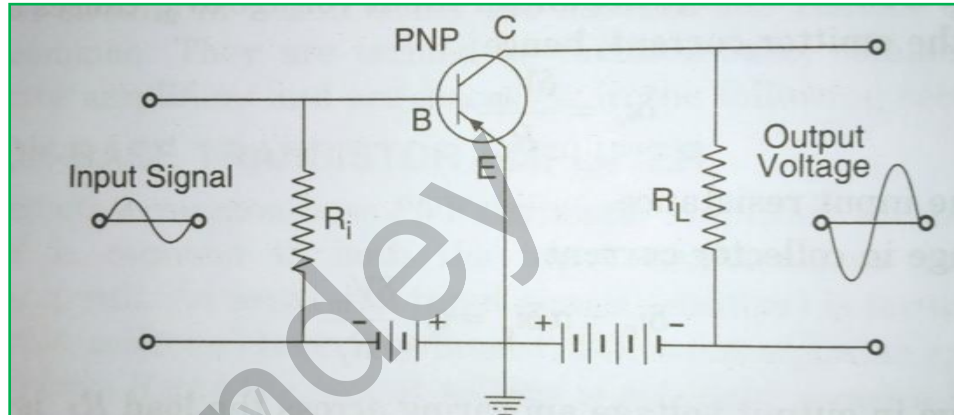


CE amplifier

$$A_i = \beta\,(ac) = \frac{\delta i_C}{\delta i_B}$$

$$A_V = \beta \frac{R_L}{R_{in}}$$

$$A_P = \beta^2 \frac{R_L}{R_{in}}$$



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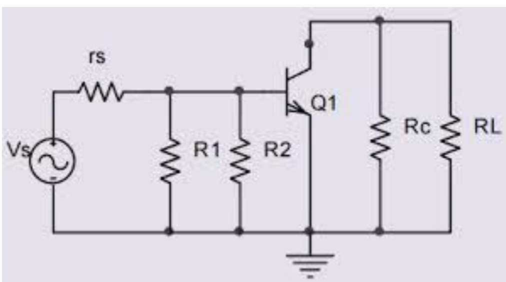
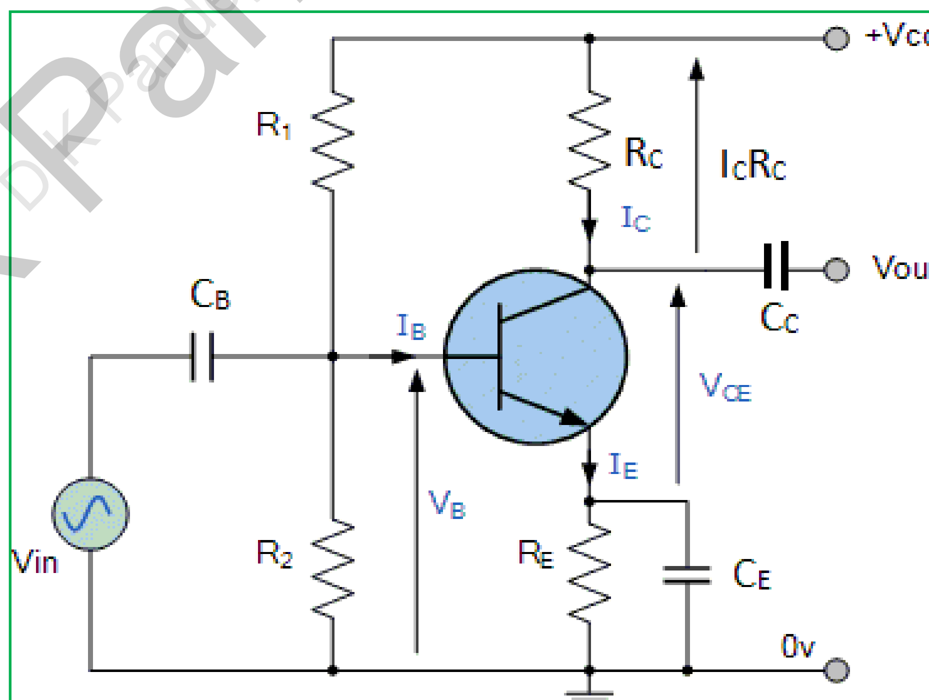




$$R_{in} = \frac{R_1 R_2}{R_1 + R_2} = \frac{\delta V_{be}}{\delta i_b}$$

$$R_{ac} = \frac{R_C R_L}{R_C + R_L}$$

$$A_V = \beta \frac{R_{ac}}{R_{in}}$$

$$A_P = \beta^2 \frac{R_{ac}}{R_{in}}$$

CE amplifier: Numerical

Example. 3. *In a single state transistor amplifier, when the signal changes by 0.02 V, the base current changes by 10 μA and collector current by 1 mA. If collector load $R_C = 2\ k\Omega$ and $R_L = 10\ k\Omega$, Calculate : (i) Current Gain (ii) Input impedance, (iii) Effective a.c. load, (iv) Voltage gain and (v) Power gain.*

Solution :

(i) Current Gain $\beta = \frac{\partial i_c}{\partial i_b}$

$$= \frac{1\ \text{mA}}{10\mu\text{A}} = 100.$$

(ii) Input impedance

$$R_i = \frac{\delta V_{BE}}{\delta i_b} = \frac{0.02}{10\ \mu\text{A}} = \mathbf{2000\ \Omega = 2}\ k\Omega$$

(iii) Effective (a.c.) load

$$R_{AC} = R_C \,||\, R_L$$
$$= \frac{R_C \times R_L}{R_C + R_L}$$
$$= \frac{2 \times 10}{2 + 10} = \mathbf{1.66\ k\Omega}$$

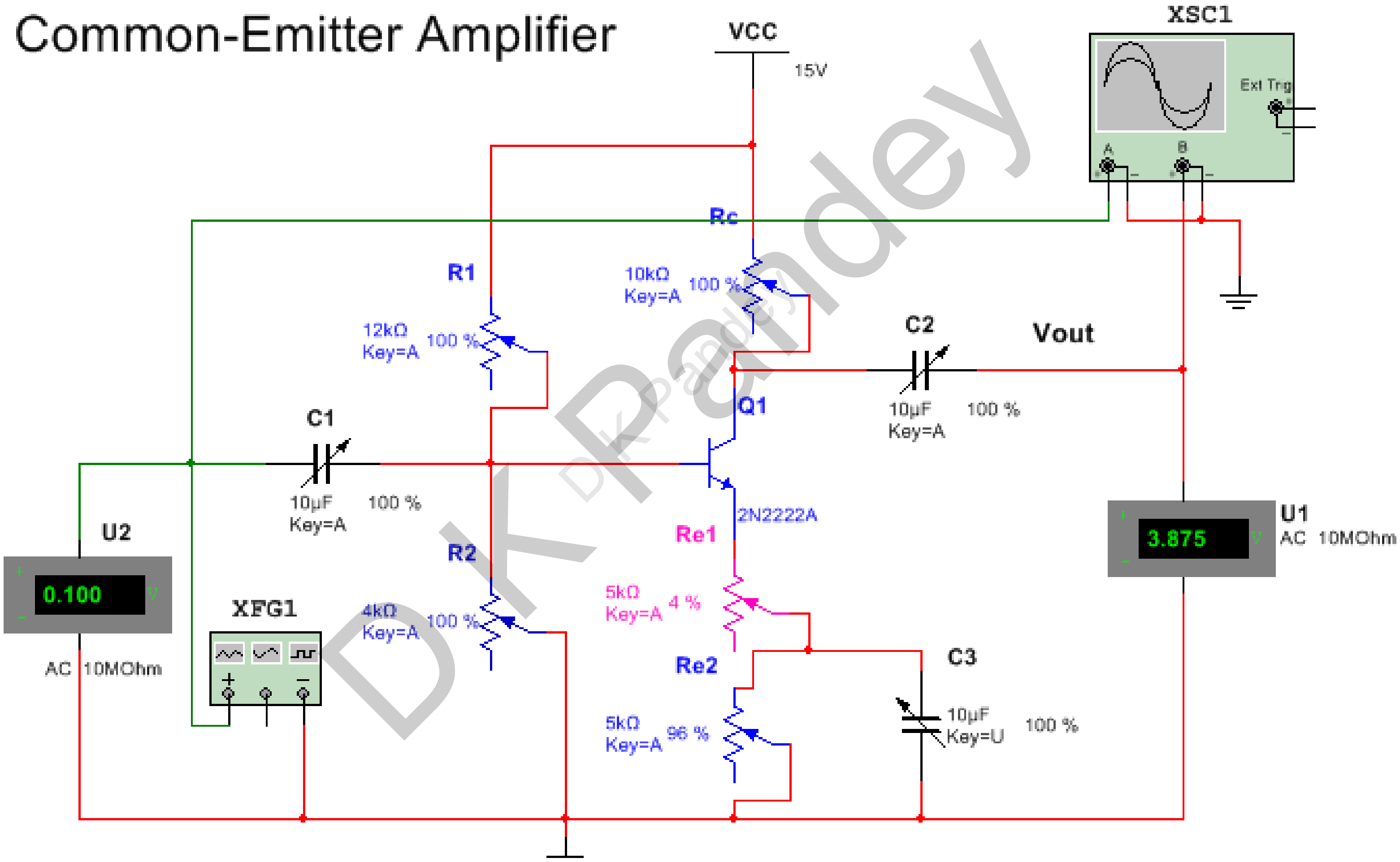
(iv) Voltage gain

$$A_v = \beta \times \frac{R_{AC}}{R_{in}} = \frac{100 \times 1.66}{2} = 83$$

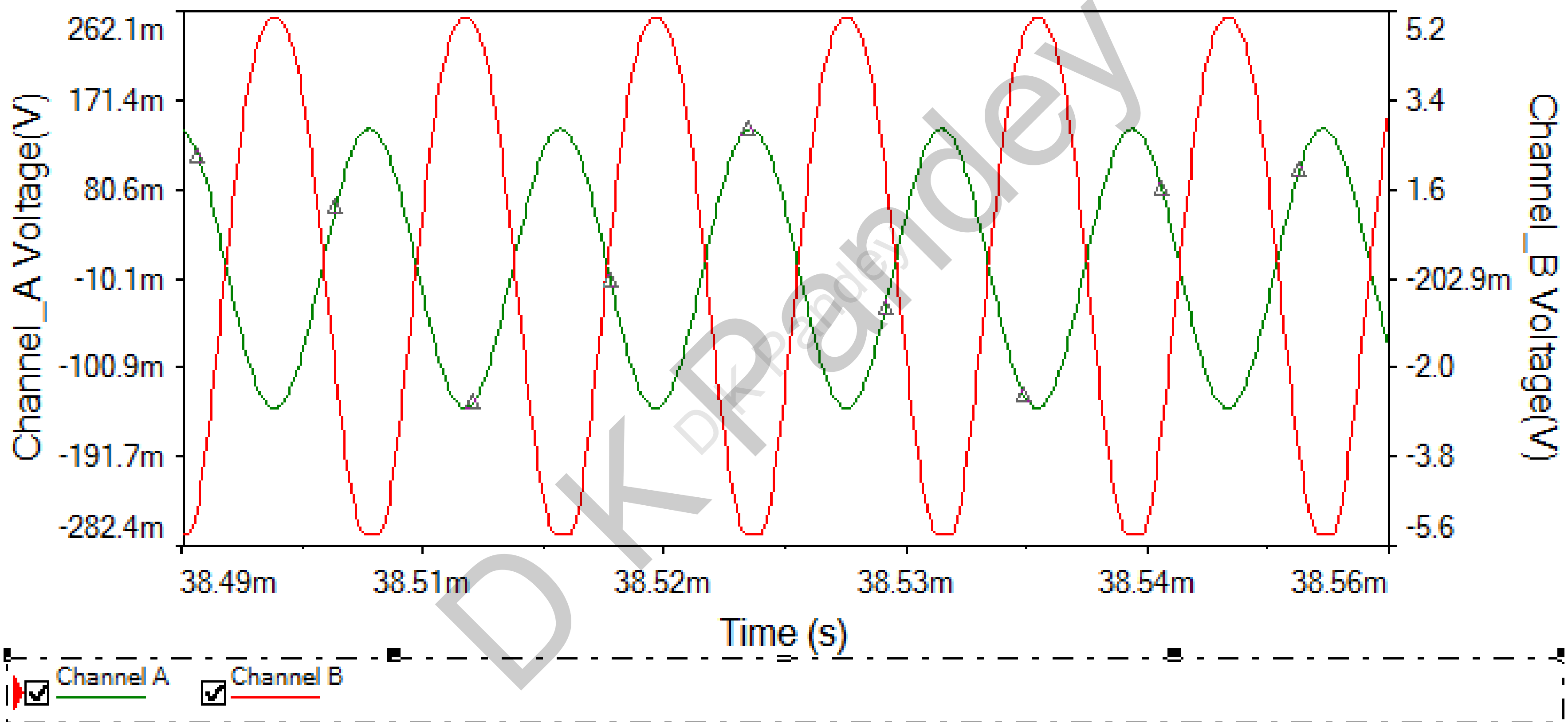
(v) Power gain, A_p = current gain × voltage gain

$$= 100 \times 83 = \mathbf{8300.}$$

CE amplifier



CE amplifier



CE amplifier : Hybrid equivalent circuit

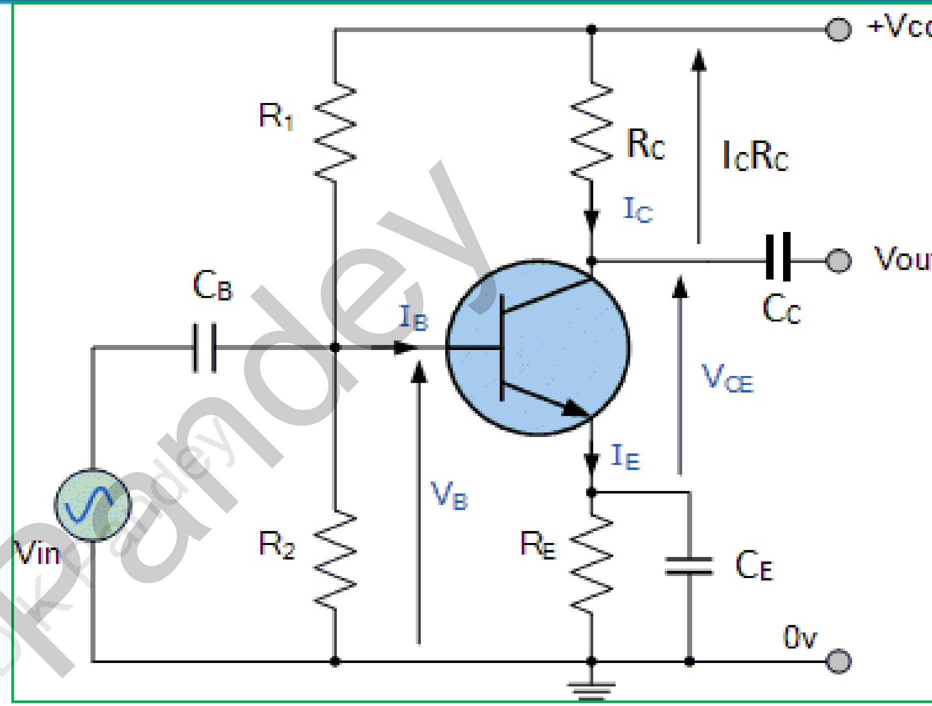
R_1 and R_2: Biasing resistance which forms potential divider to provide source (V_2=V_{Th}=V_{BB}) to input circuit.

R_C : Biasing resistance to provide appropriate source to output circuit.

R_E : Stabilization resistance.

C_B : Base capacitor which forward only ac voltage of input signal for the amplification.

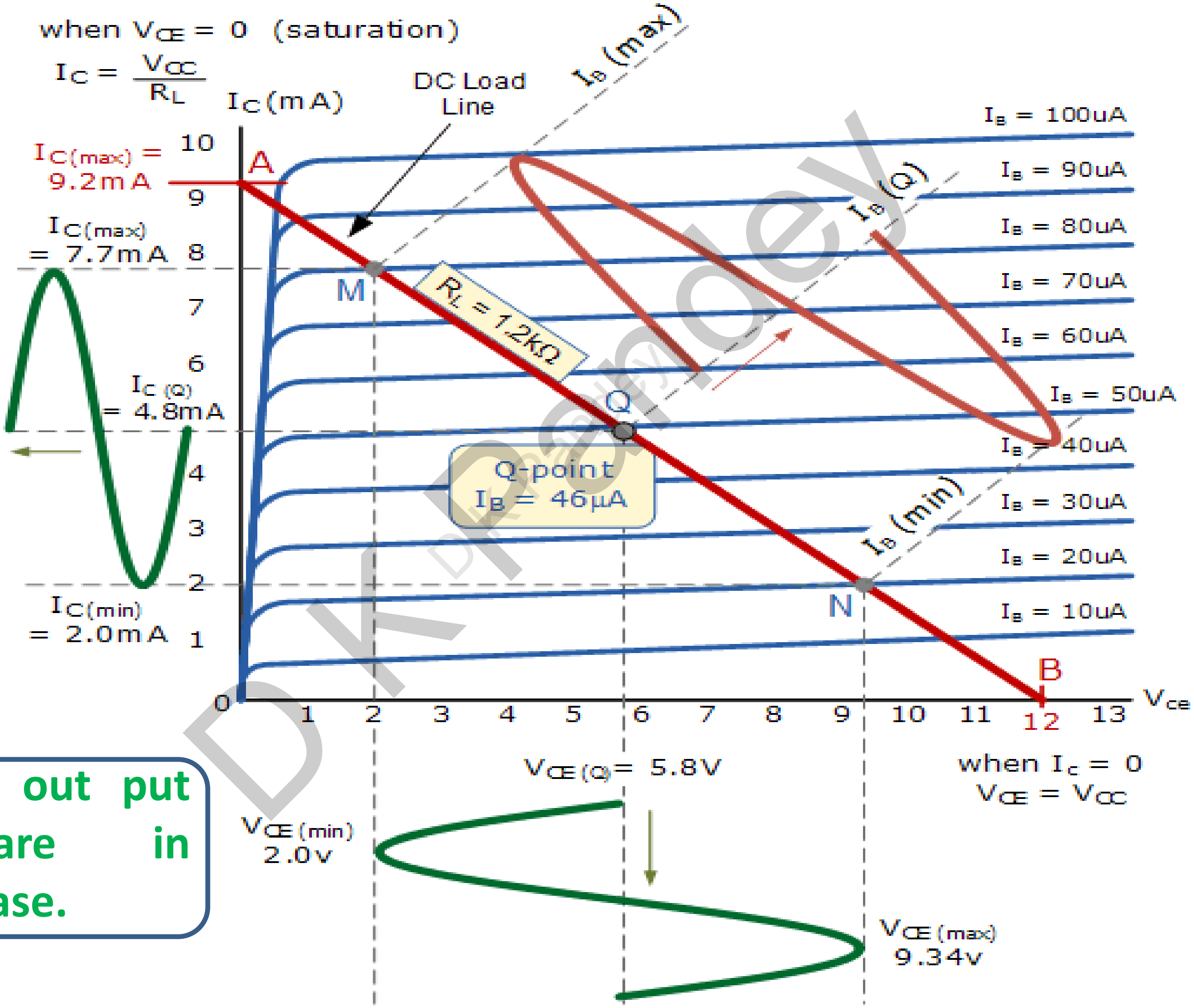
C_E : By pass capacitor which bypasses ac voltage through it to reduce the potential drop through R_E.



C_C : Collector capacitor which forwards only amplified ac voltage in output.

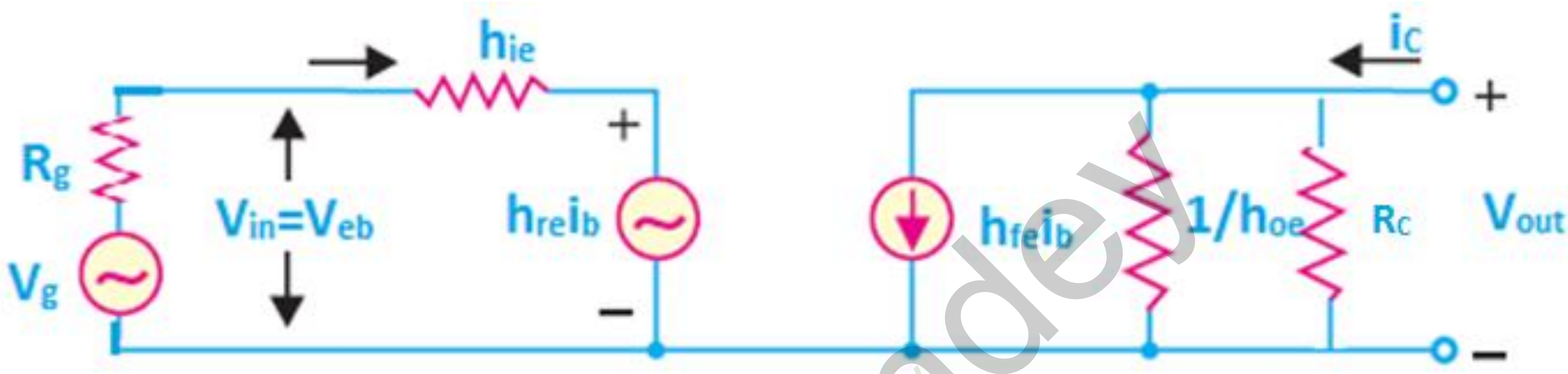
V_{CC} : Power dc source

CE amplifier hybrid equivalent circuit : Working

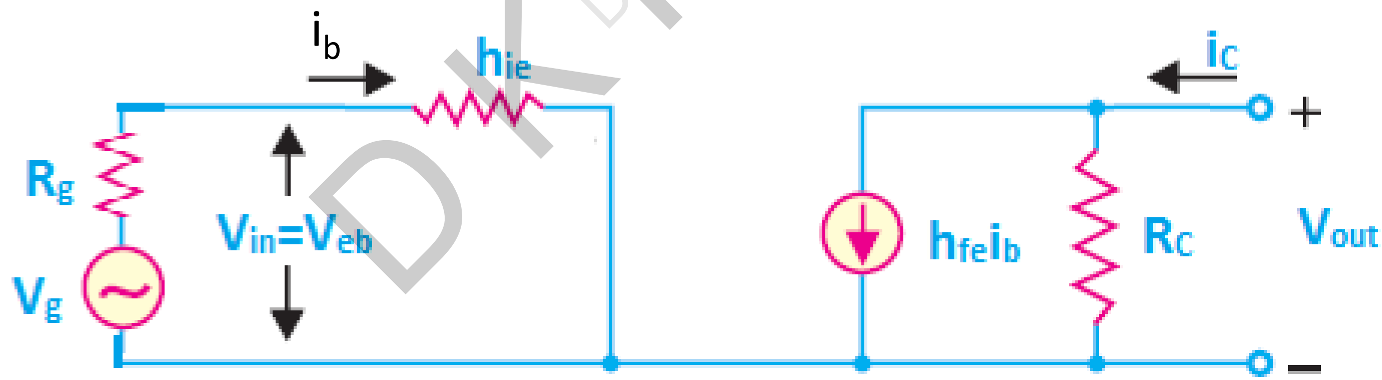


In put and out put voltage are in opposite phase.

CE amplifier hybrid equivalent circuit : Working



Since h_{re} *and* h_{oe} **has very** *small values* **therefore they can be neglected. So, simplified hybrid equivalent circuit becomes as**



CE amplifier hybrid equivalent circuit : Working

Input impedance

$$\text{Input impedance, } Z_{in} = h_{ie} - \frac{h_{re}\,h_{fe}}{h_{oe} + \frac{1}{r_L}}$$

In actual practice, the second term in this expression is very small as compared to the first term.

$$\therefore \qquad Z_{in} = h_{ie} \qquad \text{... approximate formula}$$

In the above circuit, $r_L = R_C$.

If load resistance R_L is connected across output then $r_L = R_L \parallel R_C$.

Similarly In case of potential divider biasing, The input impedance of input circuit = $h_{ie} \parallel R_B$; where $R_B = R_1 \parallel R_2$.

Output impedance

$$\text{Output impedance of transistor, } Z_{out} = \frac{1}{h_{oe} - \frac{h_{fe}\,h_{re}}{h_{ie}}}$$

The second term in the denominator is very small as compared to h_{oe}.

$$\therefore \qquad Z_{out} = \frac{1}{h_{oe}} \qquad \text{... approximate formula}$$

The output impedance of transistor amplifier

$$= Z_{out} \parallel r_L \qquad \text{where } {}^{*}r_L = R_C \parallel R_L$$

CE amplifier hybrid equivalent circuit : Working

Current gain

$$\text{Current gain, } A_i = \frac{h_{fe}}{1 + h_{oe}\, r_L}$$

In actual practice, $h_{oe}\, r_L$ is very small as compared to 1.

$$\therefore \quad A_i = h_{fe} \quad \text{... approximate formula}$$

Voltage gain

$$\text{Voltage gain, } A_v = \frac{-h_{fe}}{Z_{in}\left(h_{oe} + \frac{1}{r_L}\right)}$$

$$= \frac{-h_{fe}\, r_L}{Z_{in}\,(h_{oe}\, r_L + 1)}$$

Now approximate formula for Z_{in} is h_{ie}. Also $h_{oe}\, r_L$ is very small as compared to 1.

$$\therefore \quad A_v = -\frac{h_{fe}\, r_L}{h_{ie}} \quad \text{... approximate formula}$$

Numerical

Example 24.9. *For the circuit shown in Fig. 24.13, use approximate hybrid formulas to determine (i) the input impedance (ii) voltage gain. The h parameters of the transistor are h_{ie} = 1.94 kΩ and h_{fe} = 71.*

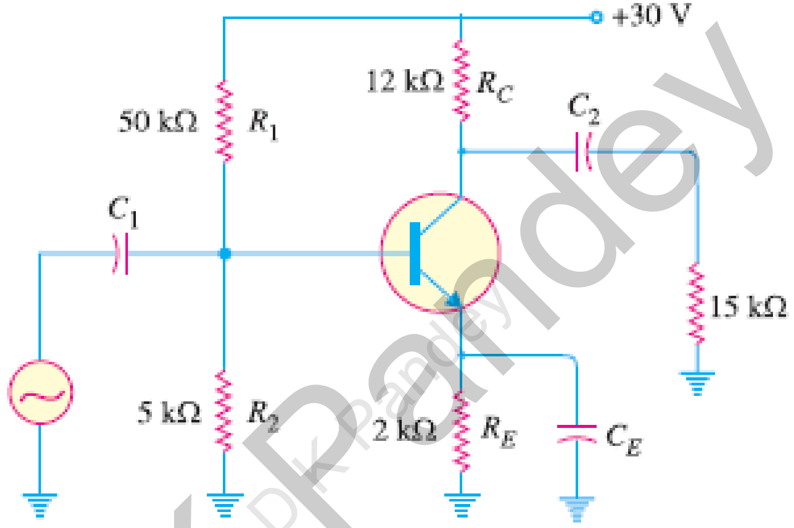


Fig. 24.13

Solution.

$$\text{a.c. collector load, } r_L = R_C \| R_L = 12\text{ k}\Omega \| 15\text{ k}\Omega = 6.67\text{ k}\Omega$$

(*i*) Transistor input impedance is

$$Z_{in\,(base)} = h_{ie} = 1.94\text{ k}\Omega$$

$$\therefore \quad \text{Circuit input impedance} = Z_{in\,(base)} \| R_1 \| R_2$$

$$= 1.94\text{ k}\Omega \| 50\text{ k}\Omega \| 5\text{ k}\Omega = \mathbf{1.35\text{ k}\Omega}$$

(*ii*)

$$\text{Voltage gain, } A_v = \frac{h_{fe}\, r_L}{h_{ie}} = \frac{71 \times 6.67\text{ k}\Omega}{1.94\text{ k}\Omega} = \mathbf{244}$$

Numerical

Example 24.11. *The following quantities are measured in a CE amplifier circuit :*

(*a*) *With output a.c. short-circuited (i.e.* $V_{ce} = 0$*)*

$$I_b = 10\ \mu A;\ I_c = 1\ mA;\ V_{be} = 10\ mV$$

(*b*) *With input a.c. open-circuited (i.e.* $I_b = 0$*)*

$$V_{be} = 0.65\ mV;\ I_c = 60\ \mu A;\ V_{ce} = 1\ V$$

Determine all the four h parameters.

Solution.

$$h_{ie} = \frac{V_{be}}{I_b} = \frac{10 \times 10^{-3}}{10 \times 10^{-6}} = \mathbf{1000\ \Omega}$$

$$h_{fe} = \frac{I_c}{I_b} = \frac{1 \times 10^{-3}}{10 \times 10^{-6}} = \mathbf{100}$$

$$h_{re} = \frac{V_{be}}{V_{ce}} = \frac{0.65 \times 10^{-3}}{1} = \mathbf{0.65 \times 10^{-3}}$$

$$h_{oe} = \frac{I_c}{V_{ce}} = \frac{60 \times 10^{-6}}{1} = \mathbf{60\ \mu mho}$$

Numerical

Example 24.5. *A transistor used in CE connection has the following set of h parameters when the d.c. operating point is V_{CE} = 5 volts and I_C = 1 mA :*

$$h_{ie} = 1700\ \Omega;\quad h_{re} = 1.3 \times 10^{-4};\quad h_{fe} = 38;\quad h_{oe} = 6 \times 10^{-6}\ \mho$$

If the a.c. load r_L seen by the transistor is 2 kΩ, find (i) the input impedance (ii) current gain and (iii) voltage gain.

Solution. (*i*) The input impedance looking into the base of transistor is

$$Z_{in} = h_{ie} - \frac{h_{re}\, h_{fe}}{h_{oe} + \frac{1}{r_L}} = 1700 - \frac{1.3 \times 10^{-4} \times 38}{6 \times 10^{-6} + \frac{1}{2000}} \simeq 1690\ \Omega$$

(*ii*) Current gain, $A_i = \dfrac{h_{fe}}{1 + h_{oe} r_L} = \dfrac{38}{1 + 6 \times 10^{-6} \times 2000} = \dfrac{38}{1.012} \simeq 37.6$

(*iii*) Voltage gain, $A_v = \dfrac{-h_{fe}}{Z_{in}\left(h_{oe} + \frac{1}{r_L}\right)} = \dfrac{-38}{1690\left(6 \times 10^{-6} + \frac{1}{2000}\right)} = 44.4$

Numerical

Example 24.7. *Find the value of current gain for the circuit shown in Fig. 24.12. The h-parameter values of the transistor are given alongside the figure.*

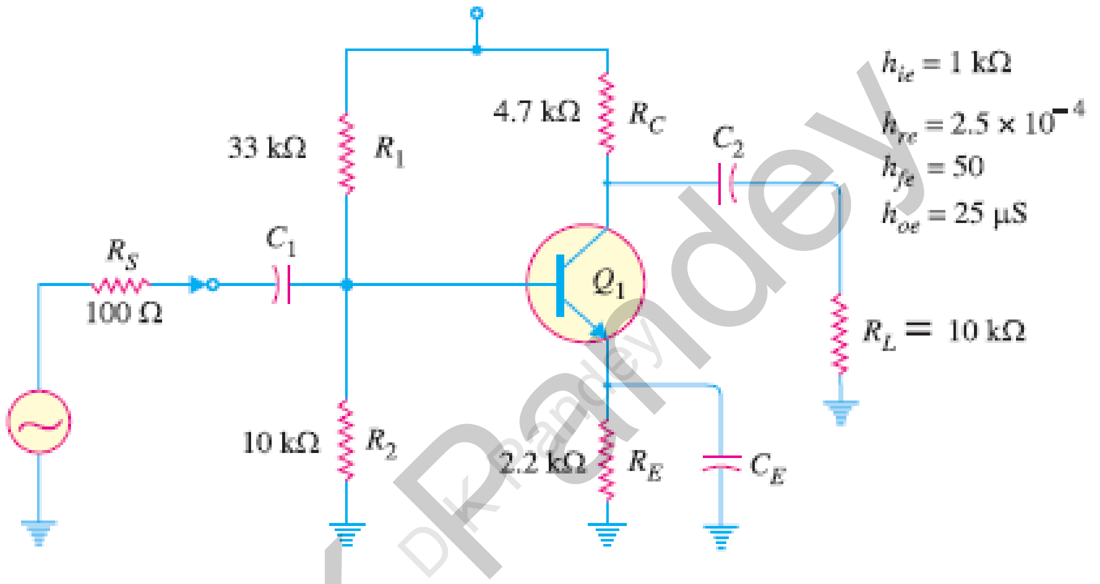


Fig. 24.12

Solution. The current gain A_i for the circuit is given by ;

$$A_i = \frac{h_{fe}}{1 + h_{oe}\, r_L}$$

$$\text{Here } r_L = R_C \,||\, R_L = 4.7\,\text{k}\Omega \,||\, 10\,\text{k}\Omega = 3.2\,\text{k}\Omega$$

$$\therefore \quad A_i = \frac{50}{1 + (25 \times 10^{-6})\,(3.2 \times 10^3)} = 46.3$$

Note that current gain of the circuit is very close to the value h_{fe}. The reason for this is that $h_{oe}\, r_L << 1$. Since this is normally the case, $A_i \simeq h_{fe}$.

Numerical

Example 24.6. *Fig. 24.11 shows the transistor amplifier in CE arrangement. The h parameters of transistor are as under :*

$h_{ie} = 1500\ \Omega;\ h_{fe} = 50;\ h_{re} = 4 \times 10^{-4};\ h_{oe} = 5 \times 10^{-5}$ ℧

Find (i) a.c. input impedance of the amplifier (ii) voltage gain and (iii) output impedance.

Solution. The a.c. load r_L seen by the transistor is equivalent of the parallel combination of R_C (= 10 kΩ) and R_L (= 30 kΩ) *i.e.*

$$r_L = \frac{R_C R_L}{R_C + R_L} = \frac{10 \times 30}{10 + 30} = 7.5\ \text{k}\Omega = 7500\ \Omega$$

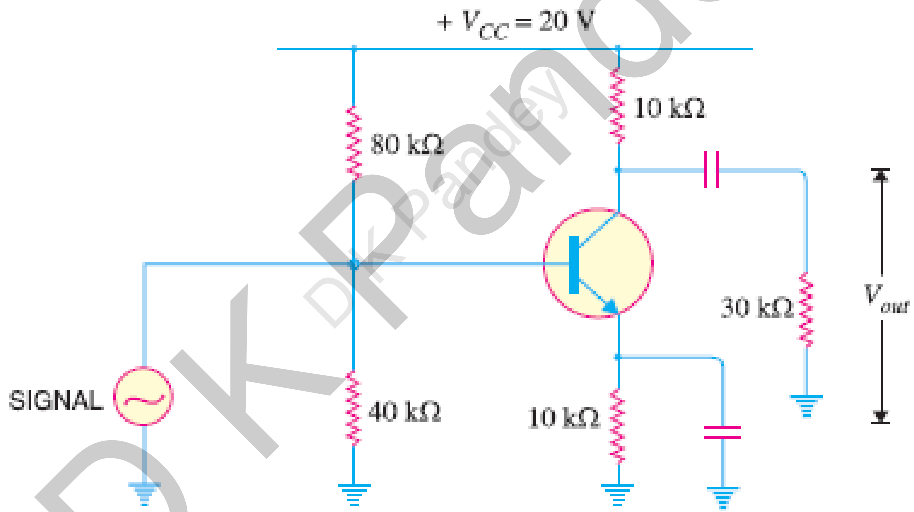


Fig. 24.11

(*i*) The input impedance looking into the base of transistor is given by :

$$Z_{in} = h_{ie} - \frac{h_{re} h_{fe}}{h_{oe} + \frac{1}{r_L}} = 1500 - \frac{4 \times 10^{-4} \times 50}{5 \times 10^{-5} + \frac{1}{7500}} = 1390\ \Omega$$

This is only the input impedance looking into the base of transistor. The a.c. input impedance of the entire stage will be Z_{in} in parallel with bias resistors *i.e.*

Numerical

Input impedance of stage = $80\times10^3 \,||\, 40\times10^3 \,||\, 1390$ = **1320 Ω**

(ii) Voltage gain, $A_v = \dfrac{-h_{fe}}{Z_{in}\left(h_{oe}+\dfrac{1}{r_L}\right)} = \dfrac{-50}{1390\left(5\times10^{-5}+\dfrac{1}{7500}\right)}$ = **– 196**

The negative sign indicates phase reversal. The magnitude of gain is 196.

(iii) Output impedance of transistor is

$$Z_{out} = \frac{1}{h_{oe}-\dfrac{h_{fe}\,h_{re}}{h_{ie}}}$$

$$= \frac{1}{5\times10^{-5}-\dfrac{50\times4\times10^{-4}}{1500}} = 27270\,\Omega = 27.27\,\text{k}\Omega$$

∴ Output impedance of the stage

$$= Z_{out}\,||\,R_L\,||\,R_C$$

$$= 27.27\,\text{k}\Omega\,||\,30\,\text{k}\Omega\,||\,10\,\text{k}\Omega = \mathbf{5.88\,k\Omega}$$

Numerical

Example 24.4. *A transistor used in CE arrangement has the following set of h parameters when the d.c. operating point is V_{CE} = 10 volts and I_C = 1 mA :*

$h_{ie} = 2000\ \Omega$; $h_{oe} = 10^{-4}$ mho; $h_{re} = 10^{-3}$; $h_{fe} = 50$

Determine (i) input impedance (ii) current gain and (iii) voltage gain. The a.c. load seen by the transistor is $r_L = 600\ \Omega$. What will be approximate values using reasonable approximations?

Solution. (*i*) Input impedance is given by :

$$Z_{in} = h_{ie} - \frac{h_{re}\, h_{fe}}{h_{oe} + \frac{1}{r_L}} = 2000 - \frac{10^{-3} \times 50}{10^{-4} + \frac{1}{600}} \qquad \text{.... (i)}$$

$$= 2000 - 28 = \mathbf{1972\ \Omega}$$

The second term in eq. (*i*) is quite small as compared to the first.

$$\therefore \qquad Z_{in} \simeq h_{ie} = \mathbf{2000\ \Omega}$$

(*ii*) Current gain,

$$A_i = \frac{h_{fe}}{1 + h_{oe} \times r_L} = \frac{50}{1 + (600 \times 10^{-4})} = \mathbf{47}$$

If $h_{oe}\, r_L << 1$, then $A_i \simeq h_{fe}$ = **50**

(*iii*) Voltage gain,

$$A_v = \frac{-h_{fe}}{Z_{in}\left(h_{oe} + \frac{1}{r_L}\right)} = \frac{-50}{1972\left(10^{-4} + \frac{1}{600}\right)} = \mathbf{-14.4}$$

The negative sign indicates that there is 180° phase shift between input and output. The magnitude of gain is 14.4. In other words, the output signal is 14.4 times greater than the input and it is 180° out of phase with the input.

Numerical

Example. 5. *The hybrid parameters of a transistor used in CE mode are $h_{ie} = 800\ \Omega$, $h_{fe} = 46$, $h_{oe} = 80 \times 10^{-6}$ mho and $h_{re} = 5.4 \times 10^{-4}$. If the effective source resistance is 500 Ω and load resistance is 5 kΩ, calculate current gain, the input resistance, the voltage gain, the output resistance and the power gain.*

(Rohilkhand 2013 Imp.)

Solution : We have

Current Gain

$$A_{ie} = \frac{h_{fe}}{1 + h_{oe} R_L}$$

$$= \frac{46}{1 + 80 \times 10^{-6} \times 5 \times 10^3}$$

$$= \mathbf{32.8}$$

Input Resistance

$$Z_{ie} = h_{ie} - h_{re} R_L A_{ie}$$

$$= 800 - 5.4 \times 10^{-4} \times 32.8 \times 5 \times 10^3$$

$$= 800 - 88.6 = \mathbf{711.4\ \Omega}$$

Voltage Gain

$$A_{ve} = \frac{A_{ie} R_L}{Z_{ie}} = 32 \cdot 8 \times 5 \times 10^3$$

$$= \mathbf{230.5}$$

Output Resistance

$$Z_{oe} = \frac{h_{ie} + R_g}{h_{oe}(h_{ie} + R_g) - h_{fe} h_{re}}$$

$$= \frac{800 + 500}{80 \times 10^{-6} (800 + 500) - 46 \times 5.4 \times 10^{-4}}$$

$$= \frac{1300}{0.104 - 0.0248}$$

$$= \mathbf{16.4\ k\Omega}$$

Power Gain

$$A_{pe} = A_{ie} \times A_{ve}$$

$$= 32 \cdot 8 \times 230.5$$

$$= \mathbf{7560.4}$$

A Lot of Thanks

for kind attention